

#### ABSTRACT OF THE DISCLOSURE

A memory device capable of suppressing reduction of a read margin resulting from fluctuation of a reference potential while reducing the area of a memory cell array 5 is obtained. This memory device comprises hysteretic capacitance means and a read circuit applying a bias voltage to the capacitance means in different directions in a first time and a second time of data reading respectively for defining read data by comparing first 10 read data and second read data with each other.